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High-Reliability Design Based on Bit-Level Repair Techniques

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ABSTRACT

Traditional memory technologies are gradually difficult to meet the demands of high-reliability applications such as automotive electronics and aerospace systems. Spin-transfer torque magnetic random-access memory (STT-MRAM) has emerged as a promising alternative due to its fast read/write speed, high endurance, and full compatibility with CMOS processes. However, the unique physical properties of STT-MRAM pose challenges including hard errors (e.g., shorts) and various types of soft errors. To address these issues, this paper proposes a high-reliability design based on bit-level repair, allowing defective bits to be repaired through dedicated conversion circuits. This approach supports both hard errors repair prior to chip fabrication and real-time repair during the product's operational lifetime, With minimal redundancy and low design complexity, the proposed method significantly improves device endurance and yield.

KEYWORDS

STT-MRAM; endurance; BIST; bit-level repair

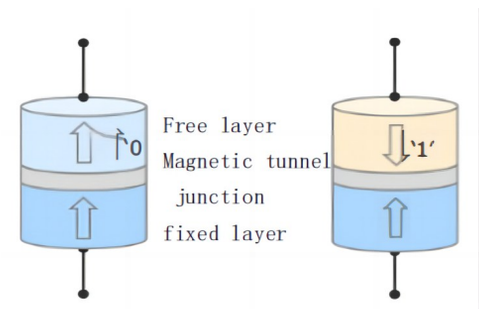
1 Introduction

Memory is a critical component of very-large-scale integrated circuits and plays a key role in determining chip yield. With the exponential growth in global data and the continuous scaling of CMOS technology, conventional memory types such as DRAM and NAND Flash face limitations in capacity, power consumption, latency, and reliability, especially for high-reliability applications. Several next-generation non-volatile memory (NVM) technologies have been developed, among which STT-MRAM stands out for its fast speed, endurance, high density, and full CMOS compatibility[1][2]. Compared to other emerging resistive memories, STT-MRAM offers superior durability[3].

Nevertheless, the distinctive characteristics of STT-MRAM—such as variability in free layer and oxide properties, state-dependent resistance distributions, and stochastic switching behavior—make it prone to hard and soft errors. Conventional repair strategies typically involve row or column redundancy, which are resource-intensive and inefficient. This paper proposes a novel circuit design that leverages bit-level repair to enhance chip reliability and yield with minimal overhead.

2 Overview of the Design

STT-MRAM is a non-volatile memory based on the spin-transfer torque effect. Its core component, the magnetic tunnel junction (MTJ), stores binary data through the magnetic alignment between its free and pinned layers. When their magnetizations are parallel, the MTJ is in a low-resistance state (P-state, storing "0"); when anti-parallel, it is in a high-resistance state (AP-state, storing "1").



(a) MTJ in a low-resistance state (b) MTJ in a high-resistance state

Fig. 1 Structure of the MTJ and its two resistance states

The bit-level repair technology identifies faulty memory cells by applying a high voltage to break them down into an irreversible breakdown state, distinguishing between the logic 0 and 1 states. During read or write operations, the chip first performs a bit-level read, then, after logical compilation based on the read bits, arranges the output or input data in sequence. Faulty bits, identified by high flags, are excluded, and replacement is performed with repaired bits. This process

ensures normal read and write operations, achieving bit-level repair functionality. The bit-level repair technology consists of four modules: the write breakdown bit module, the fault information recording module, the verification module, and the repair module. The write breakdown bit module is responsible for breaking down hard-fault bits and maintaining them in a breakdown state. The fault information recording module reads the flag bit information to distinguish normal bits from broken ones, allocates repair unit locations based on flag bit information, and outputs the location of the repair units. The verification module is responsible for checking whether the information to be written matches the information read. If they match, no rewrite is necessary. If they do not match, a write operation is required. The repair module rearranges and replaces input or output data based on the fault information. The following table shows the chip technical specifications.

Table 1 Key Technical Specifications

Parameter	Value
Operating Voltage	2.7–3.6 V
Capacity	4 Mb
Interface	SPI
Frequency	80 MHz
Endurance	1E10 cycles
Data Retention	10 years @ 85°C

3 Hardware Design

3.1 Write Breakdown Bit Module

The circuit structure of the write breakdown bit module is shown in Figure 1. The normal write operation of a bit is controlled by the Write Enable signal. In test mode, the write breakdown operation can be triggered by the combined activation of the "TM Break Enable" signal and the "Write Enable" signal.

The specific implementation is as follows:

When both the "Write Enable" and "TM Break Enable" signals are low, no operation is performed, indicating that the bit is not selected. In this state, transistors M1, M2, and M3 are all turned off.

When the "Write Enable" signal is high and the "TM Break Enable" signal is low, normal read/write operations are carried out. M1 and M2 are turned on, while M3 remains off.

When both the "Write Enable" and "TM Break Enable" signals are high, the write breakdown operation is executed. In this case, M1 is turned off, M2 is turned on, and M3 is turned on. Under this configuration, a voltage is applied across the magnetic tunnel junction (MTJ) sufficient to induce a temporary breakdown, thereby realizing the bit destruction functionality.

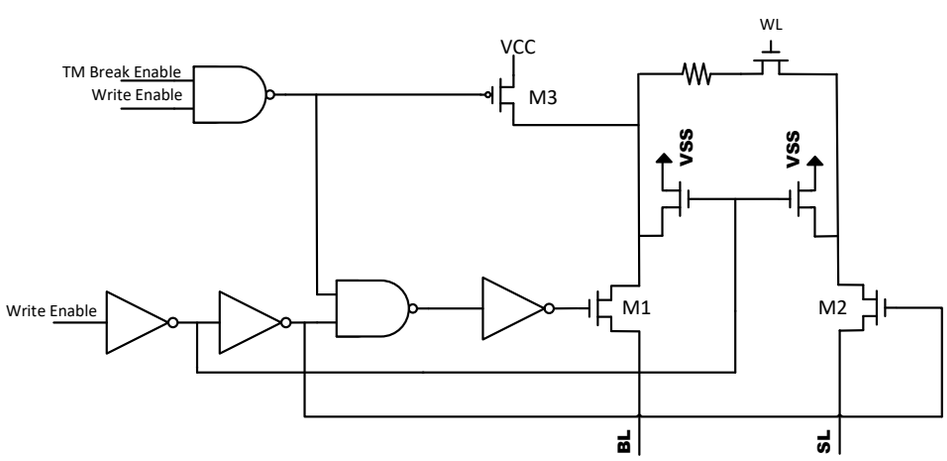


Fig. 2 Circuit Diagram of the Write Breakdown Bit Module

3.2 Fault Information Recording Module

The fault information recording module consists primarily of two parts: the flag bit information sensing circuit and the associated logic circuitry. The structure of the flag bit information sensing circuit is shown in Figure 2. It employs two voltage-mode sense amplifiers and a current mirror configuration. A reference current mirror generates three matched currents: the array current (I_{array}), the array reference current (I_{ref}), and the flag bit reference current (I_{flag}). Due to the current

mirror design, these three currents are nearly identical.

The branches carrying I_{array} and I_{ref} are connected to the first voltage-mode sense amplifier (SA1), while the branches carrying I_{array} and I_{flag} are connected to the second voltage-mode sense amplifier (SA2). In the I_{ref} branch, a reference resistor is used with a resistance value between that of the MTJ's anti-parallel state (R_{AP}) and parallel state (R_P). In the I_{flag} branch, another reference resistor is employed with a resistance value between the MTJ's breakdown resistance (R_{BD}) and its parallel state resistance (R_P). The resistance relationship satisfies:

$R_{AP} > R_P > R_{BD}$

Due to the different resistances downstream in each current branch, the node voltages at the connection points also differ. By using voltage-mode sense amplifiers, the voltages at two nodes can be compared. When the voltage at the connection point of the I_{array} branch is higher than that of the I_{ref} branch, it indicates that the resistance in the I_{array} path is greater than the reference resistor, corresponding to the MTJ's anti-parallel state (R_{AP}). Therefore, the readout result is logic '1'. Conversely, if the voltage at the I_{array} branch is lower than that of the I_{ref} branch, the resistance is less than the reference, corresponding to the parallel state (R_{AP}), and the readout result is logic '0'.

Similarly, SA2 compares the array resistance with the flag reference resistance. If the array resistance is greater than the flag reference resistance, it indicates that the bit cell is in a normal state; the output is '1', which is inverted to give Flag = 0. If the array resistance is less than the flag reference resistance, the bit is considered to be in a breakdown state; the output is '0', which is inverted to give Flag = 1.

An advantage of using voltage-mode sense amplifiers is that both comparisons can be performed simultaneously, yielding two output results. The interpretation of the outputs is as follows: (a) SA1 = 1, SA2 = 1, bit is in R_{AP} state; (b) SA1 = 0, SA2 = 1, bit is in R_P state; (c) SA1 = 0, SA2 = 0, bit is in breakdown state, The condition SA1 = 1, SA2 = 0 does not occur under normal operation.

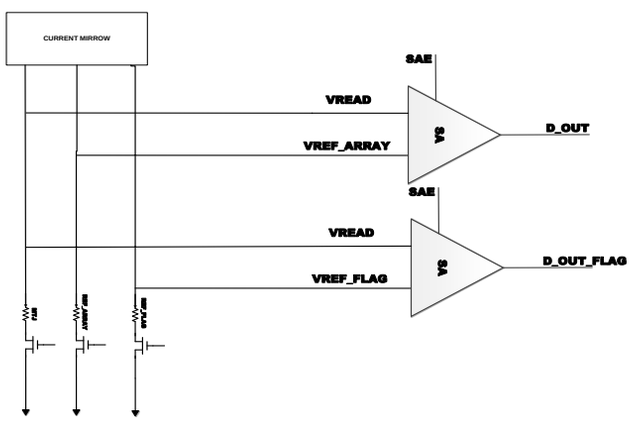


Fig. 3 Structure of the Flag Bit Information Sensing Circuit

The flag bit logic circuit consists of multiple AND gates, adders and buffers. Its main function is to process the flag data obtained from the flag bit sensing circuit. Based on the value of flag, a selection decision is made: when flag equals 1, the circuit outputs TM_REPAIR_EN = 1, indicating that a repair operation is needed. Subsequently, the corresponding spare cell is selected in sequence to perform the repair. If a spare cell itself contains a faulty bit, the circuit automatically skips that bit position and proceeds to use the next available functional bit for repair.

3.3 Verification Module

The verification module is primarily responsible for consistency checking during write operations. Its purpose is to prevent redundant write actions to bit cells where data has not changed, thereby reducing write power consumption and extending memory lifespan—particularly beneficial for non-volatile memory technologies such as STT-MRAM, which are sensitive to write energy.

When the SPI interface receives a write command along with a target address, the control logic first initiates a read operation at that address and temporarily stores the original data from the memory array. Subsequently, the SPI bus continues to receive the incoming write data from the external host. Once the complete dataset has been received, the system performs a bit-by-bit comparison between the incoming data and the original array data. If a bit in the incoming data matches the corresponding bit in the original data, a write-mask signal is generated, and no write operation is performed for that bit. If a mismatch is detected, the bit is flagged as "write-required," and the write circuitry is activated only for the changed bits.

This mechanism significantly reduces unnecessary write operations, minimizes endurance degradation of memory cells, and enhances the overall reliability and operational lifespan of the chip. Additionally, the verification module works

in conjunction with the Flag information provided by the bit-level repair module to preemptively bypass or repair faulty cells, thereby improving the correctness of the written data. The control timing diagram is shown in Figure 4.

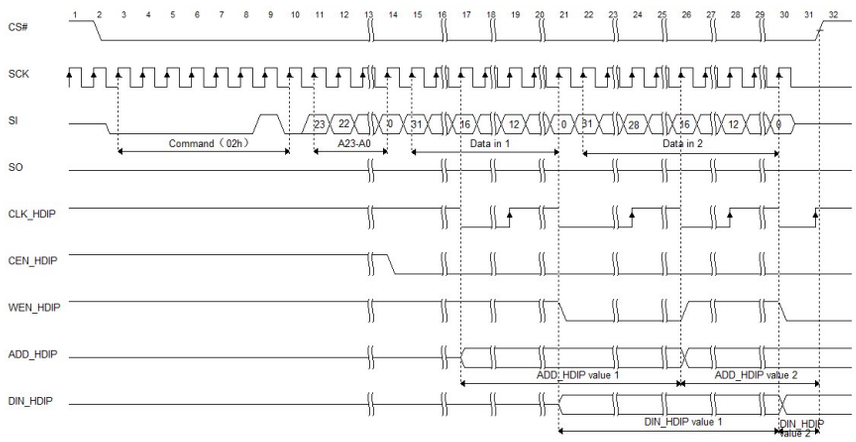


Fig. 4 Verification Timing

3.4 Repair Module

The repair module consists of two main components: an input multiplexer (Input MUX) and an output multiplexer (Output MUX), as illustrated in Figure 4. The input MUX is responsible for data input selection. It utilizes control signals TM_REPAIR_EN and TM_REPAIR_SEL to determine the data path. When TM_REPAIR_EN is low, it indicates that the corresponding input bit is not associated with a defective cell and can be written directly into the memory array. Conversely, when TM_REPAIR_EN is high, the system uses the TM_REPAIR_SEL signal to select which repair bit line should be used for data writing. All unselected input paths are considered invalid and are ignored during the write operation. The output MUX is used to select the output data path during read operations. When reading from the memory, the output MUX sequentially replaces the defective bits with the corresponding repair bits before delivering the data to the output. Similar to the input side, the output selection is governed by the TM_REPAIR_EN and TM_REPAIR_SEL signals to ensure correct data reconstruction. The detailed structure of the MUX configuration is shown in the corresponding figure.

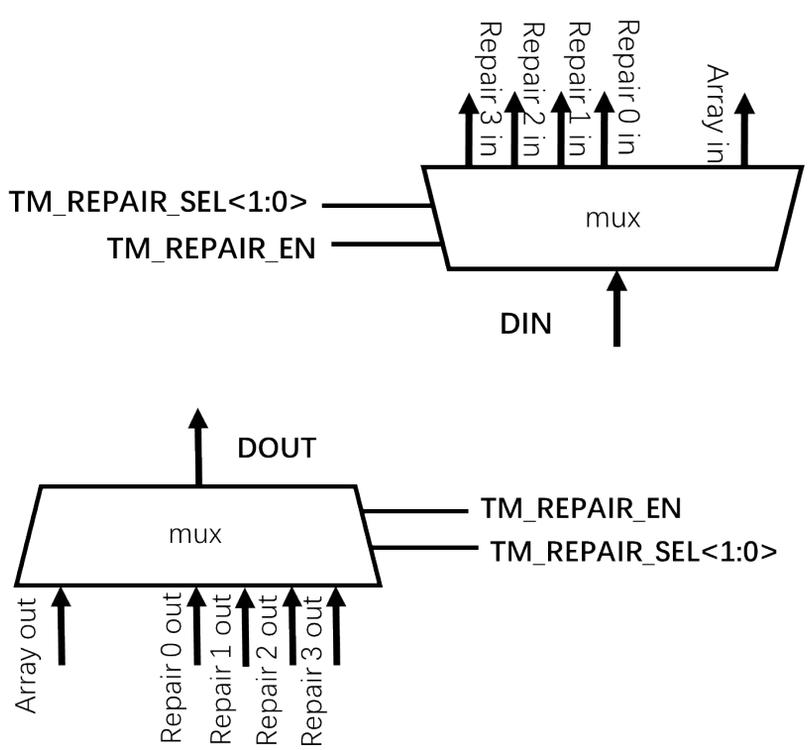


Fig. 5 (a) Input MUX Structure (b) Output MUX Structure

4 Experimental Validation

4.1 Functional Testing

The T5830ES test system was used to evaluate memory capacity, SPI interface timing, and repair capability. Data was written and read across the full 4Mb array. After enabling the repair mechanism, defective bit counts dropped to zero, verifying the effectiveness of bit-level repair.

4.2 Data Retention Testing

Accelerated aging tests at different temperatures (T1, T2, T3) were used to calculate thermal stability factors for both high- and low-resistance states. The retention time at 85°C was derived through extrapolation, confirming 10-year data stability.

4.3 Endurance Testing

Endurance failure distributions of STT-MRAM were modeled using the Weibull distribution[4].

Using voltage acceleration tests at V1, V2, and V3, characteristic lifetimes were extracted, and extrapolated to operating voltage Vop using a power-law model[5][6][7]. This predicted endurance exceeding 1E12 cycles at room temperature with a 20 ns write pulse.

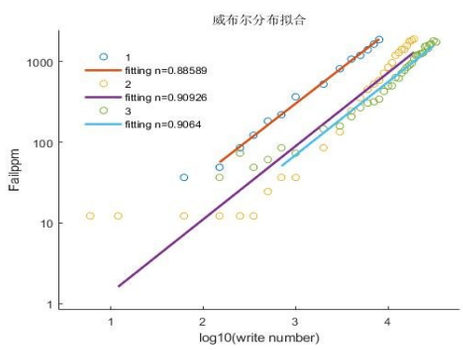


Fig. 6 Weibull Distribution Test Results of Read/Write Failures in MRAM Devices Under Three Accelerated Voltage Conditions

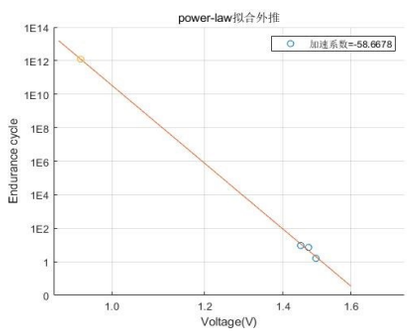


Fig. 7 Schematic Diagram of the Weibull Distribution of Read/Write Failures in MRAM Devices Under Three Accelerated Voltage Conditions

5 Conclusion

This paper proposes a robust bit-level repair strategy for STT-MRAM to address reliability challenges in high-end applications. The proposed design integrates the write breakdown bit, the fault information recording, data verification, and repair module to enable both pre-fabrication and in-field defect mitigation. The method enhances yield and reliability without significantly increasing chip area or complexity. The verification module minimizes unnecessary writes, and the bit-level repair mechanism efficiently utilizes spare resources. Experimental results under high-stress conditions demonstrate strong performance and practical potential. Future work will focus on improving the flexibility of the repair module and generalizing the repair framework to other emerging non-volatile memories such as RRAM and FRAM. This approach also offers modularity and parameter configurability, providing a scalable foundation for reliable memory design in aerospace, automotive, and other mission-critical applications.

This paper addresses the challenges of soft and hard errors in STT-MRAM under high-reliability application scenarios and proposes a bit-level repair-oriented circuit design solution. The proposed architecture integrates a write breakdown

bit module, a fault information recording module, a verification module, and a repair module, thereby enabling bit-level repair capability both before and after chip fabrication.

Without significantly increasing chip area or design complexity, this approach effectively enhances the overall yield and endurance of STT-MRAM. By introducing a verification mechanism, unnecessary write operations are significantly reduced, thereby prolonging device lifetime. The bit-level repair mechanism overcomes the inefficiencies of traditional row- or column-level redundancy, resulting in improved resource utilization. Experimental results demonstrate that the proposed repair architecture exhibits robust performance under harsh conditions, such as high temperatures and extended read/write cycles, indicating strong potential for practical engineering applications.

Future research may further improve the flexibility of the repair module and explore universal repair strategies applicable to other emerging non-volatile memories (e.g., RRAM, FRAM). This could provide new design perspectives and optimization paths for bit-level redundancy management and low-power control strategies in high-reliability chips. Moreover, the modularity and configurability of the proposed solution offer excellent scalability, supporting parameterized design and standardized interface packaging. Overall, this work presents a valuable reference architecture for next-generation high-reliability memory chips and contributes to the advancement of domestically developed and independently controllable memory technologies in critical sectors such as aerospace and automotive electronics.

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